

DEC 27 2006

Appl. No. 10/761,985  
Examiner: Tran, Thien F, Art Unit 2811  
In response to the Office Action dated September 27, 2006

Date: December 27, 2006  
Attorney Docket No. 10113681

## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

### Listing of Claims

Claims 1-18 (Canceled)

Claim 19 (Currently amended): A transistor, comprising:

a source/drain region;

a buried strap out-diffusion region adjacent to one sidewall of a deep trench; and

a bended gate structure having a bended gate and a bended gate insulating layer,

wherein the bended gate structure comprises a first portion extending along a first direction and a second portion extending along a second direction intersecting with the first direction, wherein the first portion of the bended gate is adjacent to the source/drain region and the second portion of bended gate is adjacent to the buried strap out-diffusion region, and on an overlapping region between the deep trench and bended gate structure, the sidewall profile of the deep trench comprises at least three edges.

Claim 20 (Previously presented): The transistor as claimed in claim 19, wherein the deep trench is a trench of a deep trench capacitor.

Claim 21 (Previously presented): The transistor as claimed in claim 19, wherein the bended gate is adjacent to a shallow trench isolation.

Claim 22 (Previously presented): The transistor as claimed in claim 19, further comprising a bit line contact electrically contacting the source/drain region.

Claim 23 (Previously presented): The transistor as claimed in claim 21, wherein a spacer is formed on a sidewall of the bended gate between the bit line contact and the bended gate.

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Claim 24 (Previously presented): The transistor as claimed in claim 19, wherein the bended gate is L shaped in a cross section view.

Claim 25 (Previously presented): The transistor as claimed in claim 19, wherein the bended gate insulating layer is L shaped in a cross section view.

Claim 26 (Previously presented): The transistor as claimed in claim 19, wherein the first direction and the second direction are perpendicular.

Claim 27 (Previously presented): The transistor as claimed in claim 19, wherein the source/drain region is disposed in a substrate.

Claim 28 (Previously presented): The transistor as claimed in claim 27, wherein the first direction is parallel to the substrate surface.

Claim 29 (Previously presented): The transistor as claimed in claim 19, wherein the second direction is parallel to a sidewall of the trench.

Claim 30 (Previously presented): A memory device, comprising a deep trench capacitor and a transistor controlling the deep trench capacitor, wherein the transistor is as claimed in claim 19.

Claim 31 (New): The transistor as claimed in claim 19, wherein on the overlapping region between the deep trench and bended gate structure, the sidewall profile of the deep trench comprises at least five edges.

Claim 32 (New): A memory device, comprising:

- a source/drain region;
- a buried strap out-diffusion region adjacent to one sidewall of a deep trench; and
- a bended gate structure having a bended gate and a bended gate insulating layer,

wherein the bended gate structure comprising a first portion extending along a first direction and a second portion extending along a second direction intersecting with the first direction, wherein


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the first portion of the bended gate is adjacent to the source/drain region and the second portion of bended gate is adjacent to the buried strap out-diffusion region, and on an overlapping region between the deep trench and bended gate structure, the sidewall profile of the deep trench is -shaped.